REMARKS

Claim Rejections Under 35 U.S.C. § 103

Claims 7, 8 and 12-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Sofer et al.* (U.S. Patent No. 6,643,181). Applicant respectfully traverses this rejection.

Sofer et al. discloses a method for erasing a memory cell. The method disclosed at column 2, line 63 to column 3, line 4, as cited by the Examiner, provides an erase pulse with predefined gate and drain voltages (see col. 2, lines 50 and 51). If a read operation fails at some point, the drain voltage is increased and another pulse is applied (see col. 2, lines 63 – 66). This is not the same as Applicant's claimed invention.

Applicant's invention as claimed increases the current limit of the positive voltage pulse but does not increase the pulse amplitude as disclosed by *Sofer et al.* The amount of current made available for the erase operation, is not the same as increasing the voltage level of the program pulse as in *Sofer et al.*

Additionally, Applicant's invention as claimed increases the current limit in response to the pulse count. *Sofer et al.* teaches to increase the voltage level in response to a failed read operation and only counts pulses to determine if a maximum number have been reached. Applicant is not claiming waiting for a failed read operation to increase the current limit. *Sofer et al.*, therefore, neither teaches nor suggests Applicant's claimed invention.

Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Sofer et al.* in view of *Chonan* (U. S. Patent No. 5,463,588). Please note that the Applicant's Information Disclosure Statement (IDS) incorrectly identified the patent number as "54683588" which number was repeated in the instant office action. Applicant respectfully traverses this rejection.

Chonan discloses a dynamic memory device with an internal power circuit. *Chonan* neither teaches nor suggests increasing the current limit of an erase pulse in response to the pulse count as claimed by Applicant. Therefore, even if it were obvious to combine *Chonan* with *Sofer et al.*, and Applicant maintains that it is not, the combination would not teach Applicant's invention.

Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Sofer et al.* in view of *Wooldridge* (U. S. Patent No. 6,515,909). Applicant respectfully traverses this rejection.

Wooldridge discloses a flash memory device that uses a variable length erase pulse. This neither teaches nor suggests Applicant's invention of increasing the current limit of the erase pulse in response to the number of pulses. Therefore, even if it were obvious to combine *Wooldridge* with *Sofer et al.*, and Applicant maintains that it is not, the combination would not teach Applicant's invention.

Allowable Subject Matter

Claims 10 was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

CONCLUSION

For the above reasons, Applicant respectfully requests that the Examiner withdraw the rejection and allow the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this response.

Respectfully submitted,

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